Errata Sheet

Rel. 1.5, 08.02.2008

Device	**SAK-CIC310**
Marking/Step	**EES-BA, ES-BA, BA**
Package	**PG-TQFP-64**

This Errata Sheet describes the deviations of the device from the current user documentation.

Table 1 Current Documentation

Document	Version	Date
IFLEX User's Manual	V2.1	February 2007
IFLEX Data Sheet	V2.2	June 2007

Each erratum identifier follows the pattern Module_Arch.TypeNumber:

- **Module**: subsystem, peripheral or function affected by the erratum
- **Arch**: microcontroller architecture where the erratum was firstly detected.
  - **AI**: Architecture Independent
  - **CIC**: Companion ICs
  - **TC**: TriCore
  - **X**: XC1xx / XC2xxx
  - **XC8**: XC8xx
  - **none**: C16x
- **Type**: none - Functional Deviation; '**P**' - Parametric Deviation; '**H**' - Application Hint; '**D**' - Documentation Update
- **Number**: ascending sequential number within the three previous fields. As this sequence is used over several derivatives, including already solved deviations, gaps inside this enumeration can occur.

Note: Devices marked with EES or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.

The specific test conditions for EES and ES are documented in a separate Status Sheet.

1 History List / Change Summary

Table 2 History List

Version	Date	Remark
1.0	28.07.2006	
1.1	16.02.2007	
1.2	22.06.2007	
1.3	03.08.2007	
1.4	07.09.2007	
1.5	08.02.2008	

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2 Functional Deviations

FlexRay_AI.044 Missing cycle start interrupt in startup phase

Description:

When communication is restarted by CHI command RUN after the CC left STARTUP, NORMAL_ACTIVE or NORMAL_PASSIVE state by application of CHI command READY, it may happen, that the cycle start interrupt flag `SIR.CYCS` is not set in

cycle 0 in case of a leading coldstarter

cycles 0-2 in case of an integrating node

of the following startup phase (see FlexRay Protocol Spec v2.1, fig. 7-10).

Scope:

The erratum is limited to applications where READY command is used to leave STARTUP, NORMAL_ACTIVE or NORMAL_PASSIVE state.

Effects:

Leading coldstarter: In cycle 0 of the startup phase no cycle start interrupt is generated.

Integrating node: In cycles 0-2 of the startup phase no cycle start interrupt is generated.

Workaround

Don´t leave STARTUP, NORMAL_ACTIVE or NORMAL_PASSIVE state by application of CHI command READY.

FlexRay_AI.045 Update of status register CCEV and CCSV delayed with respect to interrupt flags

Description:

A change of Error Mode, Protocol Operation Control Status and Wakeup Status sets the interrupt flags EIR.PEMC, SIR.WST, SIR.SUCS, SIR.WUPA and SIR.WUPB. The status registers are copied into the host clock domain (CCEV, CCSV) to allow read access. This clock domain crossing delays the update of the respective status fields CCEV.ERRM[1:0], CCSV.POCS[5:0] and CCSV.WSV[2:0] by up to 5 cycles of the slower of the clocks eray_bclk and eray_sclk in relation to the change of the interrupt flags.

Scope:

The erratum is limited to applications where evaluation of the status fields CCEV.ERRM[1:0], CCSV.POCS[5:0] and CCSV.WSV[2:0] is triggered by a change of one of the interrupt flags EIR.PEMC, SIR.WST, SIR.SUCS, SIR.WUPA or SIR.WUPB.

Effects:

In case the host reads the Error Mode CCEV.ERRM[1:0], the Protocol Operation Control Status CCSV.POCS[5:0] or the Wakeup Status CCSV.WSV[2:0] directly after the respective interrupt flag was set, it may happen that registers CCEV respectively CCSV are not yet updated.

Workaround

Delay reading of status fields CCEV.ERRM[1:0], CCSV.POCS[5:0] or CCSV.WSV[2:0] for at least 6 cycles of the slower of the two clocks eray_bclk and eray_sclk after the respective interrupt flag was set.

FlexRay_AI.046 Clearing of interrupt flags EIR.PEMC, SIR.WST, SIR.WUPA, SIR.WUPB, SIR.CAS, SIR

Description:

A change of POC Error Mode, Wakeup Status, reception of a Collision Avoidance Symbol or a successfully completed startup sets some of the interrupt flags EIR.PEMC, SIR.WST, SIR.WUPA, SIR.WUPB, SIR.CAS, and SIR.SUCS. Because the set condition for the respective interrupt flag may be active for up to 4 eray_bclk + 4 eray_sclk cycles, it can happen that the flag is not reset to 0_B if the host clears the flag directly after it has been set.

Scope:

The erratum is limited to applications where the interrupt flags EIR.PEMC, SIR.WST, SIR.WUPA, SIR.WUPB, SIR.CAS, SIR.SUCS are used for interrupt generation.

Effects:

In case the host clears one of the affected flags, it may happen that the interrupt stays active. A following read access will return 1_B for the respective flag.

Workaround

After clearing of one of the affected interrupt flags, the host has to reread the flag. If the flag is still set, the host has to repeat the sequence until it reads a 0_B.

FlexRay_AI.047 Clock correction value calculated with wrong deviation value

Description:

In case of receiving a valid frame after detecting an invalid frame before the action point, the clock correction value is calculated with a wrong deviation value.

Scope:

The erratum is limited to the case where an invalid frame (at least valid TSS, FSS and BSS) is detected before the action point and a valid frame, starting after the action point, is received in the same slot.

Effects:

The relative deviation (= time between secondary time reference point and action point) of the invalid frame is stored for the following rate and offset correction value calculation. This wrong deviation value may be used by the FTM algorithm to calculate the midpoint. Only in this case a wrong offset and/or rate correction value is calculated.

Workaround

None.

FlexRay_AI.048 Reception of wakeup pattern signalled for channel disconnected by SUCC1.CCHA/B

Description:

In case the CC is physically connected to a two channel network while one of the two channels is disabled by the host by programming SUCC1.CCHA/B = 0_B, the CC will signal the reception of a wakeup pattern on that channel by SIR.WST = 1_B and CCSV.WSV = 010_B (RECEIVED_WUP).

Scope:

The erratum is limited to cases where the CC is physically connected to both channels of a two channel network and one of the two channels is configured to be disconnected by the host by programming SUCC1.CCHA/B = 0_B

Effects:

Despite SUCC1.CCHA/B = 0_B the CC signals the reception of wakeup pattern on the virtually disconnected channel.

Workaround

None.

FlexRay_AI.049 Status of Network Management Vector NMVn after the CC has left NORMAL_ACTIVE orS

Description:

When the communication is restarted after the CC has left NORMAL_ACTIVE or NORMAL_PASSIVE state by application of commands READY, HALT, or FREEZE, it may happen that NMVn holds invalid data before reentering NORMAL_ACTIVE state.

Scope:

The erratum is limited to cases where NMVn is read by the host when the CC is outside NORMAL_ACTIVE or NORMAL_PASSIVE state.

Effects:

In the described case the host may read data from NMVn which originates from previous communication cycles.

Workaround

Don’t evaluate the Network Management Vector NMVn outside NORMAL_ACTIVE or NORMAL_PASSIVE state.

FlexRay_AI.050 Wrong payload data transmitted due to disturbed channel-idle sequence

Description:

If the E-Ray does not detect channel-idle (11 consecutive bit HIGH) between the end of a transmission and the beginning of the next transmission in the following transmit slot due to disturbances on the FlexRay bus, a frame with wrong payload data may be transmitted in the following transmit slot.

Scope:

The erratum is limited to the case where no channel-idle sequence is detected between two frames transmitted by the same node in two consecutive static transmit slots.

Effects:

The frame transmitted in a slot following a transmit slot with completely destroyed channel-idle sequence holds wrong payload data.

Workaround

None.

FlexRay_AI.051 Mismatch between macrotick value and cycle counter value at cycle boundary

Description:

The macrotick value `MTCCV.MTV[13:0]` is updated one eray_bclk period before the cycle counter value `MTCCV.CCV[5:0]` is updated.If a stop watch event occurs in the last macrotick of a cycle (latest 4 eray_bclk periods before cycle counter increment), the captured macrotick value `STPW1.SMTV[13:0]` and the captured cycle counter value `STPW1.SCCV[5:0]` are also mismatching.

Scope:

The erratum is limited to cases where register `MTCCV` is read one eray_bclk period before the cycle counter is incremented.For the stop watch feature the erratum is limited to the case where the stop watch event occurs in the last macrotick of a cycle (latest 4 eray_bclk periods before cycle counter increment).

Effects:

In the described cases the values of macrotick and cycle counter in register `MTCCV` and the captured values of macrotick and cycle counter in register `STPW1` may not be consistent.

Workaround

Reread register MTCCV if it was read at the end of a cycle.Consider the reduced time resolution if the stop watch was triggered at the end of a cycle.

FlexRay_AI.052 Noise following a dynamic frame that delays idle detection may fail to stop slot

Description:

If (in case of noise) the time between ’potential idle start on X’ and ’CHIRP on X’ (see FlexRay Protocol Specification v2.1, Figure 5-21) is greater than gdDynamicSlotIdlePhase, the E-Ray will not remain for the remainder of the current dynamic segment in the state ’wait for the end of dynamic slot rx’. Instead, the E-Ray continues slot counting. This may enable the node to further transmissions in the current dynamic segment.

Scope:

The erratum is limited to noise that is seen only locally and that is detected in the time window between the end of a dynamic frame’s DTS and idle detection (’CHIRP on X’).

Effects:

In the described case the faulty node may not stop slot counting and may continue to transmit dynamic frames. This may lead to a frame collision in the current dynamic segment.

Workaround

None.

FlexRay_AI.053 Content error detected in sync frame at slot boundary

Description:

In case a slot is configured for sync frame reception and a valid sync frame was received on one channel while a content error is detected exactly at the last sclk of that slot on the other channel, the valid sync frame is used for clock synchronization. For this case the FlexRay protocol specification requires that the valid frame is not used for clock synchronization (see FlexRay Protocol Specification v2.1, Fig. 6-8).If the content error on the other channel is detected at least one sclk earlier, the valid sync frame is not used for clock synchronisation (correct behaviour). If the frame on the other channel is decoded one sclk later, this results in a boundary violation, not a content error; the valid sync frame is used for clock synchronisation (also correct behaviour).

Scope:

The erratum is limited to cases where a valid sync frame is received on one channel while a frame with content error is decoded at the last sclk of the slot on the other channel.

Effects:

In the described case the valid sync frame is used for clock synchronization.

Workaround

None.

FlexRay_AI.054 Loop back mode operates only at 10 MBit/s

Description:

The looped back data is falsified at the two lower baud rates of 5 and 2.5 MBit/s.

Scope:

The erratum is limited to test cases where loop back is used with the baudrate prescaler (`PRTC1.BRP`) configured to 5 or 2.5 MBit/s.

Effects:

The loop back self test is only possible at the highest baudrate.

Workaround

Run loop back tests with 10 MBit/s (`PRTC1.BRP` = 00_B).

FlexRay_AI.055 False clock correction value possible in case action point coincides with end of received sync frame

Description:

In case the action point coincides with the end of a received sync frame, the relative deviation value (= time between secondary time reference point and action point) of this particular sync frame is seen as zero.Critical Case:When a valid sync frame is received in a specific time relation to the node's internal action point (internal signal prt_frame_decoded is high one sclk period after high pulse of gtu_action_point).Not critical when the frame is decoded one sclk before or one sclk after this critical case.

Scope:

The erratum is limited to cases where the frame length is configured to a smaller value than the action point offset and the complete frame is received between start of the slot and the slot's action point.

Effects:

In the described case a relative deviation value of zero is calculated from the received valid sync frame. This may result in a lower absolute value for the next offset and/or rate correction

Workaround

Avoid configurations with frame length smaller than action point offset.

FlexRay_AI.056 In case eray_bclk is below eray_sclk/2, TEST1.CERA/B may fail to report a detected coding error

Description:

All detected coding errors should be reported in the Test Register 1, at TEST1.CERA/ CERB. If eray_bclk is below eray_sclk/2, it may happen, depending on phase difference of eray_bclk and eray_sclk, that TEST1.CERA/ CERB are not updated in case of a detected coding error and remain in the state 0000_B = "No coding error detected".

Scope:

The erratum is limited to the case where eray_bclk is below eray_sclk/2.

Effects:

Coding errors not reported via TEST1.CERA/ CERB. The frame decoding is not affected.

Workaround

None.

FlexRay_AI.057 In case of a faulty configuration of pLatestTx and transmission across dynamic segment

Description:

Prerequisites:

- Faulty configuration of pLatestTx (MHDC.SLT) does not prevent transmission of frame X in cycle n and frame Y in cycle n+1.
- The last dynamic frame X transmitted in cycle n ends in minislot m.

Fault Case:

In case frame Y is the only frame transmitted in the dynamic segment of cycle n+1 and frame Y is transmitted across the end of dynamic segment and the last minislot of dynamic segment has the value m, error flags EIR.LTVA/ LTVB

(Latest Transmit Violation Channel A or B) are not set while EIR.TABA/ TABB (Transmission Across Boundary Channel A or B) are set as specified.

Scope:

The erratum is limited to the case where a transmission across dynamic segment boundary is not prevented because of a faulty configuration of pLatestTx (MHDC.SLT).

Effects:

In case of transmission across dynamic segment boundary the CC enters POC state HALT and the error flags EIR.TABA/ TABB are set. In case of a faulty configuration of pLatestTx the flags EIR.LTVA/ LTVB are not set.

Workaround

Configure pLatestTx as required by the FlexRay protocol specification.

FlexRay_AI.058 Wrong payload data written to receive buffer

Description:

When a receive slot is directly followed by a transmit slot and when the eray_bclk frequency is below the minimum frequency required for the configured (minislot) action point offset as listed in the table below, it may happen, that a word of the received payload is stored twice into the respective receive buffer in the Message RAM while all following words are shifted by one address and the last word is lost.With the maximum payload of 254 byte and both channels used (SUCC1.CCHA/ CCHB = 1_B) the problem may appear, depending on the configured (M)APO and TSST, if the eray_bclk is below the minimum value listed in the table below.

Table 7 fSYS_ERAY

(M)APO	min. eray_bclk, TSST=10	min. eray_bclk, TSST=3
1	63 MHz	70 MHz
2	49 MHz	53 MHz
3	40 MHz	43 MHz
4	34 MHz	36 MHz
5	30 MHz	31 MHz

APO=Action Point Offset

MAPO=Minislot Action Point Offset

In case only one channel is used (SUCC1.CCHA/ CCHB = 0_B) the values above can be multiplied by 0.66. With lower payload values the minimum eray_bclk also decreases.

Scope:

The erratum is limited to the case where eray_bclk is below a minimum frequency. This frequency depends on the configuration of GTUC9.APO, GTUC9.MAPO and PRTC1.TSST as well as on the configured payload.

Effects:

The payload of the affected receive buffer is falsified.

Workaround

Configure (M)APO and TSST according to table above depending on the used eray_bclk frequency.

FlexRay_AI.060 Generating EIR.SFO considers number of sync frames in the last cycle only, double cycle not evaluated.

Description:

In case that there are different sync IDs received for the two cycles of a double cycle and the total number of sync frames with different IDs received in the double cycle exceeds the maximum number of sync frames as configured by GTUC2.SNM while the number of sync frames within each cycle of the double cycle is below GTUC2.SNM, the sync frame overflow indication EIR.SFO is not set.

Scope:

The erratum is limited to the case where sync frames with different IDs are received in even and odd cycles and where the total number of sync frames is greater than GTUC2.SNM.

Effects:

No sync frame overflow signalled if number of received sync frames in each of the two cycles of a double cycle is below the maximum number of sync frames as configured by GTUC2.SNM.

Workaround

None.

FlexRay_AI.061 CAS collision in case of macrotick length > CAS.

Description:

A leading coldstarter that has switched from state COLDSTART_LISTEN to COLDSTART_COLLISION_RESOLUTION and that receives a CAS symbol transmitted by another coldstarter in the time window of cCASActionPointOffset (1 MT) after the state change will transmit a CAS symbol at the CAS action point. This CAS symbol should have been suppressed.

Scope:

The erratum is limited to the case where the macrotick is configured to be longer than the CAS symbol.

Effects:

A CAS collision will disturb the first cycle of the startup, delaying the startup success by one cycle.

Workaround

None.

FlexRay_AI.062 Sync frame reception after noise or aborted frame before action point

Description:

In case noise or an aborted frame leads to the detection of a secondary time reference point (STRP) and after this a valid sync frame is detected in the same slot and the STRP of the valid sync frame occures simultanoeusly with the action point, the temporal deviation value of the first detected STRP is stored instead of the value of the correct STRP.

Scope:

The erratum is limited to the case of noise before reception of a valid sync frame or a frame reception starting before action point is aborted and then a valid sync frame is received in the same slot.

Effects:

In the described case a wrong deviation value is used for correction term calculation. Depending on number of sync frames and other measured temporal deviation values it may lead to an incorrect rate or offset correction value.

Workaround

None.

FlexRay_AI.063 Additional SIR.WST events

Description:

The Status Interrupt flag SIR.WST is set not only if the status vector CCSV.WSV is changed by a protocol event, but also when the wakeup process is aborted by CHI-Commands FREEZE or READY.

Scope:

The erratum is limited to cases where a wakeup process is intentionally aborted by the Host.

Effects:

SIR.WST is set even if the status vector CCSV.WSV is not changed.

Workaround

Ignore SIR.WST after the Host intentionally aborted a wakeup process.

FlexRay_AI.066 Time stamp of the wrong channel may be used for offset correction term

Description:

In case the temporal deviation (= time between primary time reference point and action point offset) is different for channel A and B and the values have the following combination

- greater than or equal zero on one channel and negative on the other channel
- the channel with a relative deviation value greater than or equal zero is choosen for offset correction term calculation instead of the negative value.

Scope:

The erratum is limited to the case where both channels are used and if there is a large difference in the propagation delays on channel A and B.

Effects:

In case of the described relation between measured deviation values on channel A and B the calculated offset correction term may have an error of maximum the difference between the two deviation values. Thus, the error of the local time of the node is limited to the difference of the temporal deviation values of both channels.

Workaround

For dual channel FlexRay systems sync frames have to be transmitted on both channels. In practice, the propagation delay between two nodes is expected to be nearly the same on both channels. If this is not the case, the channel depending parameter pDelayCompensation[A/B] (GTUC5.DCA, DCB) has to be used to compensate the different propagation delays. With a correct adjustment of the parameter the difference of the deviation values on both channels is expected to be very low. Therefore, the error of the local time caused by the implementation error is also minimized.

FlexRay_AI.067 Reception of more than gSyncNodeMax different sync frames per double cycle

Description:

In case of receiving gSyncNodeMax or more sync frames in an even cycle, only frames with the same sync frame IDs, as received in the even cycle, may be used for offset correction term calculation in the following odd cycle.The E-Ray erroneously uses the first gSyncNodeMax sync frames for offset correction term calculation in the odd cycle, regardless whether they have been also received in the previous even cycle.

Scope:

The erratum is limited to the case where more than gSyncNodeMax nodes are configured to transmit sync frames and where different sets of sync frames are transmitted in even and odd cycle.

Effects:

In the described case the offset correction term may base on a different set of sync frames than the rate correction term. In this case registers `ESIDn` / `OSIDn` hold the IDs of the first received sync frames up to gSyncNodeMax used for offset correction term calculation.

Workaround

Avoid faulty configurations with more than gSyncNodeMax nodes configured to be transmitter of sync frames.

FlexRay_AI.068 TXEN output is undefined for even or less than 5 internal clock cycles after power on reset

Description:

The TXEN pin is set to output after power on reset. The data is derived from the corresponding register (`tx_enable_reg`) within the eray module. This register, as all ERay registers, will be reseted synchronously and gets a stable reset value, due synchronisation stages , after even or less than 5 internal clock cycles in prescaler mode.

Scope:

This erratum is limited for power on reset.

Effects:

This described case will generate a spike (low level) for even or less than 5 internal clock cycles, which is starting with the rising PORST edge.

Workaround

None.

FlexRay_AI.069 Update of Aggregated Channel Status ACS in dynamic segment in minislots following slot ID 2047

Description:

In case the slot counter has reached ID 2047 and the end of dynamic segment is not reached, the slot counter wraps around to 0 and stays there until the end of the dynamic segment. In this state (slot counter = 0) the E-Ray erroneously updates register ACS every minislot. The correct behaviour is that the slot status is only updated at the end of the dynamic segment.

Scope:

The erratum is limited to the following case: gNumberOfStaticSlots + gNumberOfMinislots > cSlotIDMax = 2047.

Effects:

In the described case register ACS is updated every minislot until the end of the dynamic segment. This update may also lead to an update of error interrupt flags EIR.EDA, EIR.EDB.

Workaround

Avoid configurations with gNumberOfStaticSlots + gNumberOfMinislots > cSlotIDMax.

FlexRay_AI.071 Faulty update of LDTS.LDTA, LDTB[10:0] due to parity error

Description:

In case a parity error occurs when the message handler transfers data from the Message RAM to the Transient Buffer it may happen, that the transmission is not started.

Scope:

The erratum is limited to cancelled transmissions of dynamic frames when a parity error occurs during data transfer from Message RAM to the Transient Buffer.

Effects:

When the described condition occurs, the slot counter value is captured and LDTS.LDTA, LDTAB[10:0] is updated with this value at the end of the dynamic segment.

Workaround

None.

FlexRay_AI.072 Improper resolution of startup collision

Description:

In case a CAS symbol is received during startup exactly at the beginning of cycle 0, the detection of following startup frames is not possible.

Scope:

The erratum is limited to the case where a CAS symbol is received during startup exactly at the beginning of cycle 0.

Effects:

In the described case the CC is not able to transit from STARTUP to NORMAL_ACTIVE state.

Workaround

Leave and re-enter STARTUP state by Host commands READY and RUN.

FlexRay_AI.074 Integration successful on X and integration abort on Y at the same point in time leads to inconsistent states of SUC and GTU

Description:

In case of ’integration successful on X’ and ’integration abort on Y’ at the same point in time, the SUC prioritizes the input event of successful integration, leaves the state INITIALIZE_SCHEDULE (CCSV.POCS) and enters (depending of its startup role) either INTEGRATION_COLDSTART_CHECK or INTEGRATION_CONSISTENCY_CHECK.

The reaction of the GTU depends on the related channels and the actual state of clock synchronisation startup process.

Assumed is that the GTU is in clock synchronization process (state CSP:A). For the combination of ’integration successful on A’ and ’integration abort on B’ the GTU stops the macrotick generation process and terminates both clock synchronisation startup processes. In this case the CC is stuck in INTEGRATION_COLDSTART_CHECK or INTEGRATION_CONSISTENCY_CHECK.

For the other combination of ’integration successful on B’ and ’integration abort on A’ the GTU stops the macrotick generation process but keeps the clock synchronisation startup process of channel A running. This leads to a delayed (best case two cycles) successful startup of the E-Ray.

If the GTU is in state CSP:B active, the same is true with the swapped channels. The combination of ’integration successful on B’ and ’integration abort on A’ leads to the stuck condition and the combination of ’integration successful on A’ and ’integration abort on B’ leads to a delayed startup.

Scope:

The erratum is limited to the case of simultaneous generation of internal signals ’integration successful on X’ on one channel and ’integration abort Y’ on the other channel.

Effects:

In the described cases the E-Ray either is stuck in startup states or extends the startup by at least two cycles.

Workaround

Use a timer to measure how long the E-Ray stays in state INTEGRATION_COLDSTART_CHECK or INTEGRATION_CONSISTENCY_CHECK. If the timeout is reached, re-enter the startup state by using the CHI commands READY and RUN.

FlexRay_AI.075 Detection of parity errors outside immediate scope

Description:

The protocol engine reads at least the first two words of its Transient Buffer and one word more than required by the payload count for each transmitted message, even if no data is needed (null frame or payload count is zero). If a parity error is detected when the protocol engine reads from the Transient Buffer, the transmitted message is invalidated by setting its CRC code to zero.

Scope:

The erratum is limited to the case where a parity error occurs in one of the words in the Transient Buffer that are read but not needed for a particular message.

Effects:

The transmitted message is invalidated.

Workaround

None.

FlexRay_AI.076 CCSV.SLM [1:0] delayed to CCSV.POCS[5:0] on transitions between states WAKEUP and READY.

Description:

When the POC state changes between WAKEUP and READY the content of register CCSV may show a slight discontinuity, i.e. CCSV.SLM [1:0] may be updated late.

Scope:

The erratum is limited to configurations with SUCC1.TSM = 0_B (ALL Slot Mode).

Effects:

None, CCSV.SLM [1:0] only relevant in POC states NORMAL_ACTIVE and NORMAL_PASSIVE.

Workaround

Ignore CCSV.SLM [1:0] in states READY and WAKEUP.

FlexRay_AI.077 Wakeup listen counter started one bit time early

Description:

If the protocol engine is in the state WAKEUP_LISTEN and if the parameter gdWakeupSymbolRxLow is programmed to a value 11-n, then the channel idle recognition CHIRP comes n bit times early.

Scope:

The erratum is limited to configurations with gdWakeupSymbolRxLow < 11. Bit rates of 10/5/2.5 MBit/s requires a minimum gdWakeupSymbolRxLow of 46/23/11 gdBit.

Effects:

The wakeup pattern is transmitted n bit times early.

Workaround

Set gdWakeupSymbolRxLow to value >= 11.

FlexRay_AI.078 Payload corruption after reception of valid frame followed by slot boundary crossing frame

Description:

If after reception of a valid frame in slot N the reception of a second frame (transmitted by a miss synchronized node) starts in the same slot and the payload of the second frame is stored into the TBF shortly after the slot boundary, the first 32 bit payload data of the first received frame in the TBF is overwritten by the payload data from the second frame.

Scope:

The erratum is limited to cases where the complete header and a part of the payload of another frame is received in slot N.

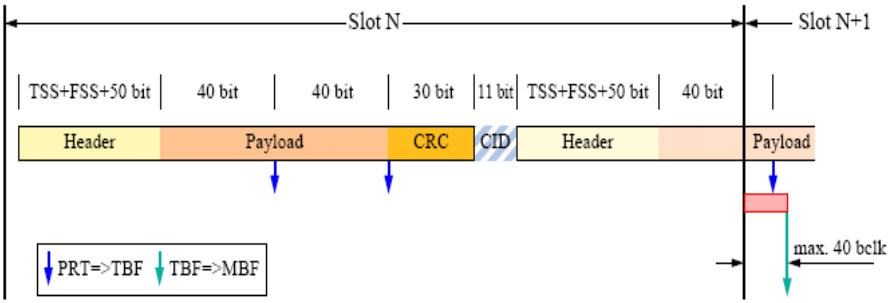

Figure 1 The second frame starts in the same slot

The transfer of a received valid frame from TBF to MBF is initiated by the end of the actual slot. Execution is started not later than 40 bclk periods after the slot change. 40 bclk periods equate 10 bit times, when bclk=40MHz. Corruption of payload occurs when a transfer from PRT to TBF happens in the red marked time window between start of new slot and start of transfer from TBF to MBF.

Effects:

The first two words (4 byte) of the received valid frame's payload are corrupted.

Workaround

1. Ensure that the static slot length is configured suited to the static payload length.
2. Check Message Buffer Status for boundary violation.

FlexRay_AI.079 `CCSV.RCA[4:0]` and `CCSV.PSL[5:0]` inconsistent after FREEZE command.

Description:

When the FREEZE command is applied during STARTUP it may happen, that after the command `CCSV.RCA` and `CCSV.PSL` are inconsistent.

Scope:

The erratum is limited to cases where the FREEZE command coincides with a protocol triggered state change where `CCSV.RCA[4:0]` is decremented.

Effects:

`CCSV.RCA [4:0]` is decremented but `CCSV.PSL[5:0]` does not show state COLDSTART_COLLISION_RESOLUTION.

Workaround

Ignore `CCSV.RCA[4:0]` after CHI command FREEZE.

FlexRay_AI.080 CLEAR_RAMS command does not clear the 1st RAM word

Description:

After execution of the CLEAR_RAMS command, the 1st RAM word holds the last data written to IBF. Reason is that the registers to support byte access to the RAM are cleared one clock cycle after the CLEAR_RAMS command was started.

Scope:

The erratum is limited to cases where the CLEAR_RAMS command is applied during E-Ray operation. The execution of the CLEAR_RAMS sequence after hard reset is not affected.

Effects:

Execution of the CLEAR_RAMS command does not reset the first word of an E-Ray internal RAM to zero.

Workaround

Write 0x00000000 to any address of IBF directly before applying CLEAR_RAMS command.

FlexRay_AI.082 After detecting low level beyond gdWakeupSymbolRx-Window, the node may complete

Description:

In case of a WUP that starts with a duration at the LOW level that is longer than (n*gdWakeupSymbolRxWindow) but shorter than (n*gdWakeupSymbolRxWindow + gdWakeupSymbolRxLow), followed by a duration of at least gdWakeupSymbolRxIdle at the HIGH level and followed by a duration of at least gdWakeupSymbolRxLow at the LOW level, the last part of this received within a window with a duration of at most gdWakeup-SymbolRxWindow, then this WUP is detected as valid while it should be considered invalid.

Scope:

The erratum is limited to cluster wakeup with disturbances on a channel.

Effects:

Detection of WUP is independent of WakeupSymbolRxWindow's phase.

Workaround

None.

FlexRay_AI.083 Irregular sync frame list exported in state Coldstart_Gap

Description:

If the protocol engine is in the state Coldstart_Gap, it stops transmitting its own startup frame (according to the protocol specification), but the status data exported to the CHI (`SFS`, `OSIDn` register) lists its own startup-frame as transmitted.

Scope:

The erratum is limited to leading coldstart nodes.

Effects:

Misleading status data.

Workaround

Ignore misleading status data in state Coldstart_Gap.

FlexRay_AI.084 Corruption of frame received in slot N by second frame reception before action point

Description:

If a receive slot N is followed by a transmit slot N+1, and if between end of frame reception in slot N and start of frame transmission in slot N+1 the reception of a frame (transmitted by a mis-synchronized node) is started, it may happen, that header and/or payload of the valid frame received in slot N is corrupted.

Case1: Frame reception completed in slot N.

Case2: Frame reception across slot boundary between slot N and slot N+1.

Case3: Frame reception starts in slot N+1.

Scope:

The erratum is limited to the case where a receive slot is followed by a transmit slot and where at least the complete header of another frame is received before the frame received in slot N has been stored into the respective message buffer.

Effects:

Case1: Syntax error signalled for slot N, correct behaviour, no corruption.

Case2: Boundary violation signalled for slot N and slot N+1. Header and/or payload of the message buffer assigned to slot N may be corrupted or frame received in slot N may be completely rejected.

Case3: No error signalled for slot N. Frame received in slot N may be not stored or header of the message buffer assigned to slot N may be corrupted. Corruption of the assigned message buffer's payload may only occur when eray_bclk is below 25 MHz.

Workaround

None.

FlexRay_AI.085 Cycle filtering in slot 1

Description:

The message buffer for slot 1 is searched in parallel to every scan in the previous cycle. A message buffer scan is started every 8th slot. A running scan is aborted if the NIT is reached. The message buffer used for slot 1 depends on the cycle filter configuration and the bus activity in the dynamic segment. If the scan is aborted between the first and the last message buffer assigned to slot 1, it is unpredictable, if the correct message buffer is used.

Scope:

The erratum is limited to the case where two (or more) message buffers are configured for slot 1 and cycle filtering is used.

Effects:

If a running message buffer scan is interrupted by the NIT it cannot be guaranteed that the correct message buffer is used for transmission in slot 1 of the next cycle.

Workaround

If cycle filtering is used, assign all message buffers configured for slot 1 to the static buffers section. I.e. message buffer number < `MRC.FDB[4:0]`.

MLI_TC.007 Answer frames do not trigger NFR interrupt if `RIER.NFRIE`=10_B and Move Engine enabled

If `RIER.NFRIE`=10_B, a NFR interrupt is generated whenever a frame is received but, if Move Engine is enabled (`RCR.MOD`=1_B, "automatic mode"), the NFR interrupt is suppressed for read/write/base frames. However, this interrupt is actually also supressed for answer frames, which are not serviced by Move Engine.

Workaround

To trigger NFR interrupts for read answer frames, having Move Engine enabled, then:

- Set RIER.NFRIE=00_B when no read is pending.
- Set RIER.NFRIE=01_B when a read is pending. Any read/write/base/answer frame will trigger the NFR interrupt. Then, by reading RCR.TF in the interrupt handler, it can be detected whether the received frame was the expected answer frame or not.

SSC_AI.020 Writing SSOTC corrupts SSC read communication

Programming a value different from 0 to register SSOTC if SSC module operates in Slave Mode corrupts the comunication data.

Workaround

Don't program SSOTC different from 0 in Slave Mode.

SSC_CIC.008 Move engine returns always 0 at MRST during write operation

In case of a write operation the SSC move engine returns always 0 at MRST instead of the address and written data.

Workaround

No recommendation.

SSC_CIC.009 SSC master mode is not implemented

SSC master mode is not implemented in the current design.

Workaround

None.

SSC_TC.009 SSC_SSOTC update of shadow register

The beginning of the transmission (activation of SLS) is defined as a trigger for a shadow register update. This is true for SSOC and most Bits of SSOTC, but not necessarily for Bits 1 and 0 (Leading Delay), since the decision, whether leading cycles have to be performed, has to be made before.

The current implementation does not take the actual SSCOTC values into account (i.e. if trailing and/or inactive cycles have to be performed and would allow a later update), but performs the update just before the earliest possible occurrence of a leading cycle. This means the update of SSOTC(1:0) is done at the end of the last shift cycle of the preceding transmission.

Workaround

If during a continuous transmission the value for SSOTC.LEAD has to be changed, the update of SSOTC has to be done before the transmission is completed (internal trigger for receive interrupt) in order to get valid timely for the next transmission.

SSC_TC.011 Unexpected phase error

If SSCCON.PH = 1 (Shift data is latched on the first shift clock edge) the data input of master should change on the second shift clock edge only. Since the slave select signals change always on the 1st edge and they can trigger a change of the data output on the slave side, a data change is possible on the 1st clock edge.

As a result of this configuration the master would activate the slave at the same time as it latches the expected data. Therefore the first data latched is might be wrong.

To avoid latching of corrupt data, the usage of leading delay is recommended. But even so a dummy phase error can be generated during leading, trailing and inactive delay, since the check for a phase error is done with the internal shift clock, which is running during leading and trailing delay even if not visible outside the module.

If external circuitry (pull devices) delay a data change in slave_out/master_in after deactivation of the slave select line for n*(shift_clock_perid/2) then a dummy phase error can also be generated during inactive delay, even if SSCCON.PH = 0.

Workaround

Don't evaluate phase error flag SSCSTAT.PE. This is no restriction for standard applications (the flag is implemented for test purpose).

TOP_CIC.002 80 MHz clock at XTAL not possible

With BYPASS=0 the oscillator is in power down mode but the shaper is not bypassed. Therefore an external 80 MHz clock signal at XTAL1 is not propagated into the chip and the chip is not running.

Workaround

None.

3 Deviations from Electrical- and Timing Specification

FlexRay_CIC.P001 ERAY interface timing

The values d10Bit_TX (t_{60}) and d10Bit_RX (t_{63}) are not subject to production test, verified by design/characterization.

FlexRay_CIC.P002 RXDA/RXDB Signal Timing at end of frame

For the current step of the CIC310 the following ERAY timing values are valid:

Table 8 ERAY Interface Timing (Operating Conditions apply)**;** C_L = 35 pF

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
time span between last BSS and FES that can to be properly decoded without influence of external quartz circuitry tolerances (d10Bit_Rx)[1)2)]	t_{63}	SR	966,43	1046.03	ns
RxD capture by f_{sample} (RxDA/RxDB => sampling flip-flop) (dRxAsym)[1)2)3)]	$\|t_{64}-t_{65}\|$	CC	-	3.45	ns

1) Not subject to production test, verified by design/characterization.
2) f_{oscdd} = 20 MHz or 40 MHz; C_L = 35 pF; PRT.BRP = 0; PRT.SPP = 0; (RxDA, RxDB); External noise on V_{DDAPLL} : Amplitude <= 10 mV, Frequency <= 200 kHz
3) Asymmetrical delay of rising and falling edge (RxDA, RxDB).

Footnote 2 is also valid for ERAY interface timing $|t_{61}-t_{62}|$ in the data sheet.

MLI_CIC.P001 MLI interface timing

For the current step of the CIC310 the following MLI timing values are valid:

Table 9 MLI Interface Timing (Operating Conditions apply); C_L = 50 pF

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
TCLK clock period	t_{40}	CC/SR	T_{MLI} 1)	-	ns
TCLK high period	t_{41}	CC	45%	55%	t_{40}
TCLK low period	t_{42}	CC	45%	55%	t_{40}
RCLK high period	t_{41}	CC	20%	80%	t_{47}
RCLK low period	t_{42}	CC	20%	80%	t_{47}
TDATA and TVALID valid after TCLK rising edge	t_{45}	SR	0%	28%	t_{40}
RVALID and RDATA setup to RCLK falling edge	t_{46}	SR	10%	-	t_{47}
RVALID and RDATA hold from RCLK falling edge	t_{48}	SR	10%	-	t_{47}

1) $t_{MLImin} = 2 \times T_{SYS} = 2 \times 1/f_{sys}$. When f_{SYS} = 80 MHz, t_{40} = 25 ns

All MLI timing values described in the data sheet except t_{41} and t_{42} are related to the minimum value T_{MLI}.

SSC_CIC.P001 Minimum value of the DIR lead delay timing t_{28}

The minimum value of the DIR lead delay timing t_{28} to the SCLK rising edge (`CON.PO`, `CON.PH` =00_H) and SCLK falling edge (`CON.PO`, `CON.PH` = 10_H) is 8ns.

TOP_CIC.P001 Minimum value of active mode core supply current I_{DD}

The minimum value of the active mode core supply current I_{DD} is 3mA. This applies to the condition f_{sample} = 80MHz, f_{sample}/f_{sys} = 1:1 and f_{sample} = 80MHz, f_{sample}/f_{sys}=2:1.

TOP_CIC.P002 Pad output rise/fall time matching

The definition of the rise/fall time matching in the current data sheet is only valid for a 50 pF capacitive load at the Class A2 Pad output.

The values of the pad output rise/fall time matching described in the data sheet are not subject to production test, verified by design/characterization.

TOP_CIC.P003 Accumulated PLL jitter

The PLL causes a jitter of f_{PLL} and affects all clocks derived form the PLL clock. There will be defined two formulas that define the (absolute) approximate maximum value of the jitter D_p in ns with a K-factor K=6, the f_{PLL}=80 MHz and the number P of consecutive f_{PLL}.

$D_p[ns] = ((334{,}08 * P) / (f_{sample}^2 [MHz] * K)) + 0.065$ with P < 50, K = 6, f_{sample} = 80 MHz, f_{OSCDD} = 20MHz or 40 MHz

$D_p[ns] = 0{,}5$ with P > 50, K = 6, f_{sample} = 80 MHz, f_{OSCDD} = 20MHz or 40 MHz

The maximum peak-to-peak noise on the supply voltage pin V_{DDAPLL} is limited to a peak-to-peak voltage of V_{PP}=10mV and frequency less than 200 KHz.

TOP_CIC.P004 V_{OLA} / V_{OHA} definition using medium driver

The output low voltage V_{OLA} (operating conditions as defined in data sheet for DC characteristics) is max. 0.4V with I_{OL}=1.4 mA for medium driver mode.

The output high voltage V_{OHA} (operating conditions as defined in data sheet for DC characteristics) is min. 2.4V with I_{OH}=1.4 mA for medium driver mode.

XTAL_CIC.P001 XTAL shaper bypass is not functional

The electrical parameters of the input low voltage V_{ILX}, input high voltage V_{IHX}, input clock high time, input clock low time, input clock rise time and input clock fall time at XTAL1 are only valid with XTAL shaper in bypass.

In the current design the XTAL shaper bypass is not functional and the electrical parameters with XTAL shaper in bypass are not applicable.

4 Application Hints

FlexRay_AI.H002 Timer 1 Precision

The relative timer is used to generate timing triggers based on the Macrotick counter. If activated (set bit `T1C.T1RC`), the timer waits for the first Macrotick increment signal to start its configured Macrotick counting. This leads to an uncertainty of one Macrotick in single-shot mode and for the first period in continuous mode.

For subsequent counting periods in continuous mode this kind of uncertainty does not occur and the precision of the timer signal increases to a single bclk cycle.

Workaround

None.

MLI_TC.H005 Consecutive frames sent twice at reduced baudrate

If frames are transmitted back to back it may happen that transmitted frames are not acknowledged at the first transmission and the transmitter will automatically repeat the transmission. Therefore all frames except the first one are sent twice. No data will be lost.

The problem takes place if the MLI transmit clock is divided by more than a factor of two with respect to the system clock, which means the baudrate is not maximum.

Workaround

1. Set transmit clock to maximum frequency ($f_{SYS}/2$).
2. Insert a delay between transmission of two consecutive frames.

MLI_TC.H006 Deadlock situation when MLI_TCR.RTY=1

The MLI module offers optionally a `Retry` functionality. It is aimed at ensuring data consistency in case blocks of data have to be transferred by a `dumb` move engine which can not react to MLI interrupt events.

If MLI_TCR.RTY = 1_B, any requesting bus master will retry the request (read or write) until it is accepted by the MLI module.

Under certain circumstances (specific access sequence on the bus in conjunction with a non responding MLI partner, etc), this may result in a deadlock situation, where no instruction can be executed anymore.

In this case also interrupts cannot be processed anymore. The deadlock can only be resolved by a reset.

Workaround

Always disable automatic retry mechanism by writing MLI_TCR.RTY = 0_B.

The `Retry` functionality is actually not needed in any application. The MLI interrupt events (transmit interrupt, etc.) are sufficient to ensure data consistency, and therefore should be used to trigger the wanted interrupts, DMA transfers, etc.

SSC_CIC.H002 SSC access to 32 bit register

Using the SSC interface only 16 bit accesses are possible and all 32 bit accesses are splitted into two 16 bit accesses being performed one after another. Therefore special care has to be taken when accessing registers with complex dependencies (e.g. lock of register T0C by setting timer run bit).

Workaround

Split accesses to registers with complex dependencies in 16 bit accesses and keep a reasonable order of accesses (e.g. first write upper halfword of T0C register to configure Timer 0 Macrotick Offset and start T0 afterwards by writing lower halfword of T0C register).

SSC_CIC.H003 No direct changes of the SSC configuration register SSC_CON.PH and SSC_CON.PO with the SSC Move Engine

Direct changes of the SSC configuration register SSC_CON.PH and SSC_CON.PO with the SSC Move Engine (external SSC access) leads to undefined behavior.

Workaround

To change the SSC configuration register SSC_CON.PH and SSC_CON.PO, stop the SSC communication and change the SSC configuration register with the DMA.

SSC_CIC.H004 Prefetch by consecutive SSC read

By consecutive SSC read (with auto increment) of address n to address m an internal prefecht to address m+2 is done. Is the address m+2 outside of the specification, a bus error can occur.

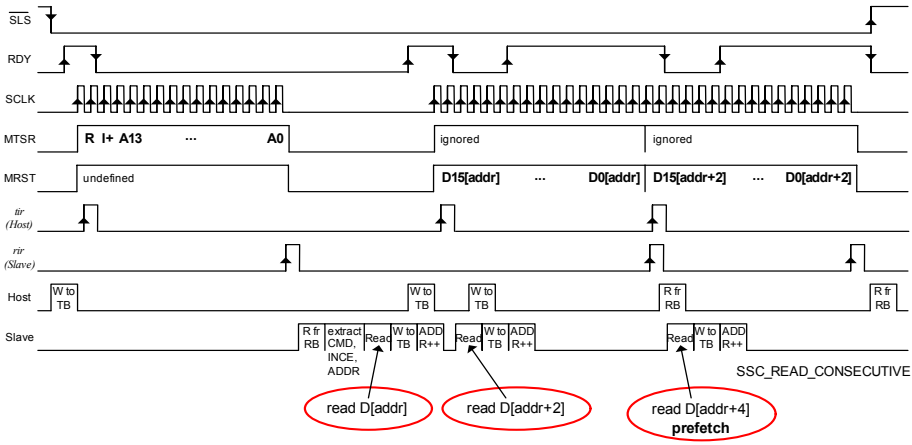

Figure 2 SSC READ CONSECUTIVE

Workaround

Accesses to address ranges outside of the specification are not allowed.

TOP_CIC.H001 Access to an undefined address range leads to undefined behavior

Accesses to reserved address ranges or address ranges outside of the specification are not allowed. They may lead to an undefined behavior.

Workaround

It is forbidden to access address ranges that are not specified.

5 Documentation Updates

TOP_CIC.D001 Address line mapping of the XMU interface in JTAG enable mode

The address line mapping of the XMU interface in JTAG enable mode is not implemented, but described in the specification chapter 8.7.2 “External Address Extension“.

Workaround

None.

TOP_CIC.D002 Wrong interrupt connection to P0.9

The implementation of the int_o1 and int_o0 connection is different to the description in the current documentation.

In the current documentation is written for P0.9:

ALT2 INT_O0

ALT3 INT_O1

The connection for P0.9 is implemented:

ALT2 INT_O1

ALT3 INT_O0

Workaround

None.

TOP_CIC.D003 The stop watch event ERAY_STPWT is not triggered via input pin.

The stop watch event ERAY_STPWT is not triggered via input pin. The function is not available.

Workaround

None.

TOP_CIC.D004 DMA trigger logic

In the current specification each DMA channel has an input multiplexer to select one input trigger source for the activation of programmed move operation(s). This assignment is not implemented in the current design. The implementation is described in the following figure DMA channel logic.

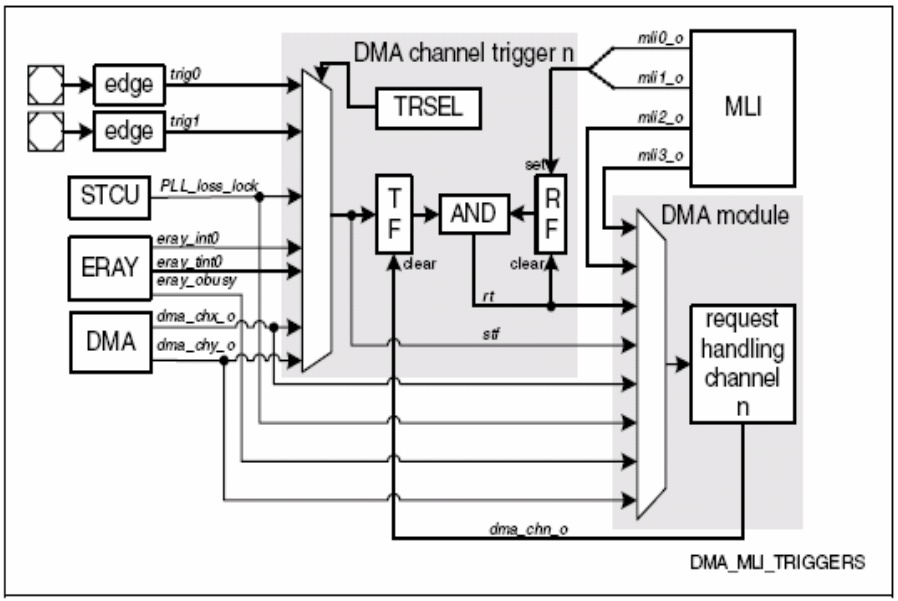

Figure 3 DMA channel logic (only for DMA channel 00)

Workaround

None.

TOP_CIC.D005 DMA PRSEL trigger matrix

The description of the DMA request assignment matrix in the specification is not implemented in the current design step. The DMA request input lines of the DMA are implemented according to the following table:

Table 10 DMA Request Assignment

DMA Channel	DMA Request Input	DMA Request Source	Selected by
00	ch07_out	DMA channel 07	CHCR00.PRSEL=000_B
	ch06_out	DMA channel 06	CHCR00.PRSEL=001_B
	mli2_o	MLI	CHCR00.PRSEL=010_B
	mli3_o	MLI	CHCR00.PRSEL=011_B
	rt	Ready Flag RF	CHCR00.PRSEL=100_B
	stf	Trigger Flag TF	CHCR00.PRSEL=101_B
	eray_obusy	E-RAY Transfer Message RAM to Output Buffer RAM busy	CHCR00.PRSEL=110_B
	PLL_loss_lock	PLL Unlocked	CHCR00.PRSEL=111_B
01	ch00_out	DMA channel 00	CHCR01.PRSEL=000_B
	ch07_out	DMA channel 07	CHCR01.PRSEL=001_B
	mli2_o	MLI	CHCR01.PRSEL=010_B
	mli3_o	MLI	CHCR01.PRSEL=011_B
	rt	Ready Flag RF	CHCR01.PRSEL=100_B
	stf	Trigger Flag TF	CHCR01.PRSEL=101_B
	eray_obusy	E-RAY Transfer Message RAM to Output Buffer RAM busy	CHCR01.PRSEL=110_B
	eray_ibusy	E-RAY Transfer Output Buffer RAM to Message RAM busy	CHCR01.PRSEL=111_B

Table 10 DMA Request Assignment

DMA Channel	DMA Request Input	DMA Request Source	Selected by
02	ch01_out	DMA channel 01	CHCR02.PRSEL=000_B
	ch00_out	DMA channel 00	CHCR02.PRSEL=001_B
	mli2_o	MLI	CHCR02.PRSEL=010_B
	mli3_o	MLI	CHCR02.PRSEL=011_B
	rt	Ready Flag RF	CHCR02.PRSEL=100_B
	stf	Trigger Flag TF	CHCR02.PRSEL=101_B
	eray_obusy	E-RAY Transfer Message RAM to Output Buffer RAM busy	CHCR02.PRSEL=110_B
	eray_ibusy	E-RAY Transfer Output Buffer RAM to Message RAM busy	CHCR02.PRSEL=111_B
03	ch02_out	DMA channel 02	CHCR03.PRSEL=000_B
	ch01_out	DMA channel 01	CHCR03.PRSEL=001_B
	mli2_o	MLI	CHCR03.PRSEL=010_B
	mli3_o	MLI	CHCR03.PRSEL=011_B
	rt	Ready Flag RF	CHCR03.PRSEL=100_B
	stf	Trigger Flag TF	CHCR03.PRSEL=101_B
	eray_obusy	E-RAY Transfer Message RAM to Output Buffer RAM busy	CHCR03.PRSEL=110_B
	eray_ibusy	E-RAY Transfer Output Buffer RAM to Message RAM busy	CHCR03.PRSEL=111_B

Table 10 DMA Request Assignment

DMA Channel	DMA Request Input	DMA Request Source	Selected by
04	ch03_out	DMA channel 03	CHCR04.PRSEL=000_B
	ch02_out	DMA channel 02	CHCR04.PRSEL=001_B
	mli2_o	MLI	CHCR04.PRSEL=010_B
	mli3_o	MLI	CHCR04.PRSEL=011_B
	rt	Ready Flag RF	CHCR04.PRSEL=100_B
	stf	Trigger Flag TF	CHCR04.PRSEL=101_B
	eray_obusy	E-RAY Transfer Message RAM to Output Buffer RAM busy	CHCR04.PRSEL=110_B
	eray_ibusy	E-RAY Transfer Output Buffer RAM to Message RAM busy	CHCR04.PRSEL=111_B
05	ch04_out	DMA channel 04	CHCR05.PRSEL=000_B
	ch03_out	DMA channel 03	CHCR05.PRSEL=001_B
	mli2_o	MLI	CHCR05.PRSEL=010_B
	mli3_o	MLI	CHCR05.PRSEL=011_B
	rt	Ready Flag RF	CHCR05.PRSEL=100_B
	stf	Trigger Flag TF	CHCR05.PRSEL=101_B
	eray_obusy	E-RAY Transfer Message RAM to Output Buffer RAM busy	CHCR05.PRSEL=110_B
	eray_ibusy	E-RAY Transfer Output Buffer RAM to Message RAM busy	CHCR05.PRSEL=111_B

Table 10 DMA Request Assignment

DMA Channel	DMA Request Input	DMA Request Source	Selected by
06	ch05_out	DMA channel 05	CHCR06.PRSEL=000_B
	ch04_out	DMA channel 04	CHCR06.PRSEL=001_B
	mli2_o	MLI	CHCR06.PRSEL=010_B
	mli3_o	MLI	CHCR06.PRSEL=011_B
	rt	Ready Flag RF	CHCR06.PRSEL=100_B
	stf	Trigger Flag TF	CHCR06.PRSEL=101_B
	eray_obusy	E-RAY Transfer Message RAM to Output Buffer RAM busy	CHCR06.PRSEL=110_B
	eray_ibusy	E-RAY Transfer Output Buffer RAM to Message RAM busy	CHCR06.PRSEL=111_B
07	ch06_out	DMA channel 06	CHCR07.PRSEL=000_B
	ch05_out	DMA channel 05	CHCR07.PRSEL=001_B
	mli2_o	MLI	CHCR07.PRSEL=010_B
	mli3_o	MLI	CHCR07.PRSEL=011_B
	rt	Ready Flag RF	CHCR07.PRSEL=100_B
	stf	Trigger Flag TF	CHCR07.PRSEL=101_B
	eray_obusy	E-RAY Transfer Message RAM to Output Buffer RAM busy	CHCR07.PRSEL=110_B
	eray_ibusy	E-RAY Transfer Output Buffer RAM to Message RAM busy	CHCR07.PRSEL=111_B

Workaround

None.

TOP_CIC.D006 External service request signal matrix

The current specification describes the assignment of the external service request signal matrix. This assignment is not implemented in the current design. The current implementation is described in the following figure:

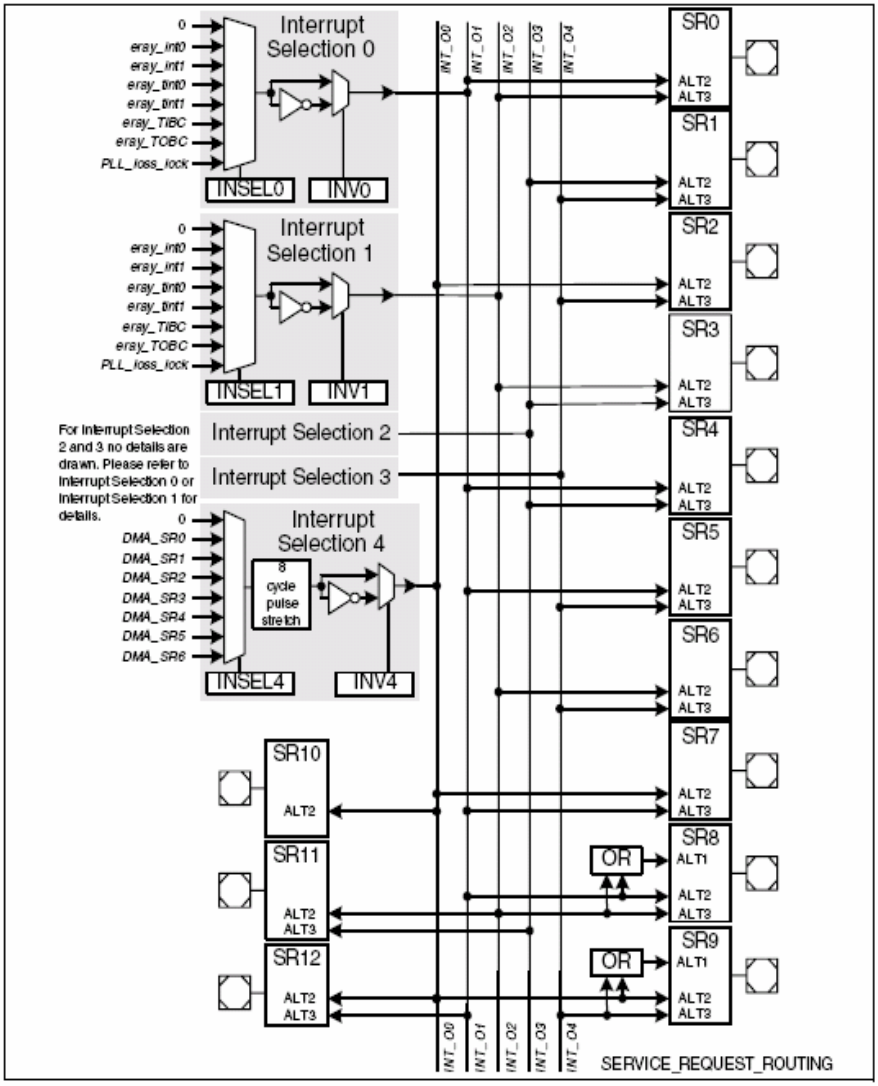

Figure 4 Service Request Routing

Workaround

None.

TOP_CIC.D007 SSC ME interrupt disable

The current specification describes the disable control of the SSC ME interrupt request by the SYSCON register bit 25, DISME. Furthermore the specification describes the connection of the ssc_tir and ssc_rir flags to the DMA. This functionality is not implemented in the current design. Bit 25 in SYSCON register is a reserved register.

Workaround

None.

TOP_CIC.D014 Initialization of the Service Request Pin SR8/SR9

The current User's Manual describes in chapter 10.1.5 and 10.3.5 "The Initialization Values of the Service Request Control" the assignment of the PLL_loss_lock event to the service request pin SR8 by the Initialization Move Engine (IME). The PLL_loss_lock event assignment to a SR pin is controlled by SRCR.INSEL1, which routed the internal interrupt signal to **INTO2** and not to INTO1.

The current User's Manual describes in chapter 10.2.5 "The Initialization Values of the Service Request Control" the assignment of the PLL_loss_lock event to the service request pin SR9 by the Initialization Move Engine (IME). The PLL_loss_lock event assignment to a SR pin is controlled by SRCR.INSEL0, which routed the internal interrupt signal to **INTO1** and not to INTO0.